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Before the Board of Patent Appeals and Interferences

In re the Application

Inventor	:	SATOH
Application No.	:	09/830,376
Filed	:	04/25/2001
For	:	A DATA WRITING/READING METHOD, A DE-INTER-LEAVING METHOD, A DATA PROCESSING METHOD, A MEMORY AND A MEMORY DRIVE APPARATUS

APPEAL BRIEF

On Appeal from Group Art Unit 2188

Date: 07/16/2007

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Michael Ure
(Name)

M Ure 7/16/07
(Signature and Date)

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TABLE OF CASES

NONE

I. REAL PARTY IN INTEREST

The real party in interest is NXP B.V., the successor in interest to the present assignee of record of the present application, Koninklijke Philips Electronics N.V., and not the party named in the above caption.

II. RELATED APPEALS AND INTERFERENCES

With regard to identifying by number and filing date all other appeals or interferences known to Appellant which will directly effect or be directly affected by or have a bearing on the Board's decision in this appeal, Appellant is not aware of any such appeals or interferences.

III. STATUS OF CLAIMS

Claims 1, 3, 4, 6, 7, 9 and 10-18 are pending, all of which stand finally rejected and form the subject matter of the present appeal. Claims 2, 5 and 8 have been canceled.

IV. STATUS OF AMENDMENTS

All amendments have been entered. No amendment after final rejection has been submitted.

V. SUMMARY of the CLAIMED SUBJECT MATTER

The present invention relates to the transfer of data to and from memory, particularly for purposes of de-interleaving. In a conventional data de-interleaver, data is written in one direction (row or column) and read in a an opposite direction (row or

column) in such a manner as to reverse a previously-performed interleaving operation. Doubling-buffering is typically performed. In a double-buffered de-interleaver, as data is being read from one memory, new data is being written to another memory. The roles of the two memories are switched back and forth. Data throughput is thereby increased. This double-buffering requirement increases system cost.

The present invention reduces system cost by using a single-buffering arrangement in such a way that reading and writing can occur substantially simultaneously in a non-interfering way. Instead of switching the roles of two memories back and forth, the direction of reading from and writing to a single memory is alternated back and forth in such as way that after reading of a portion (row or column) of the memory has been completed, writing of that same portion of the memory can be begun.

The following analysis of independent claim 1 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
1. A data writing/reading method of sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that	Figs. 4-6	
a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction,	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
a second plurality of data	Figs. 4-6, esp. Fig. 5	Data written in the row

being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction;		direction (Fig. 4) is read out in the column direction; when the first column has been read out, it is over-written by succeeding data (Fig. 5). This manner of operation progresses until all of the data have been read out in the column direction and over-written by new data (Fig. 6). See page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.

The following analysis of independent claim 4 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
4. A method of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that	Figs. 4-6	
a first plurality of data is	Figs. 4-6	Page 15, line 30 to page 16,

written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction,		line 3; page 18, lines 1-14; page 19, lines 8-20.
a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction;	Figs. 4-6, esp. Fig. 5	Data written in the row direction (Fig. 4) is read out in the column direction; when the first column has been read out, it is over-written by succeeding data (Fig. 5). This manner of operation progresses until all of the data have been read out in the column direction and over-written by new data (Fig. 6). See page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.

The following analysis of independent claim 7 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
7. A data processing method comprising a first step of interleaving a plurality of data, and a second step of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that	Figs. 4-6	
a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction,	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction;	Figs. 4-6, esp. Fig. 5	Data written in the row direction (Fig. 4) is read out in the column direction; when the first column has been read out, it is over-written by succeeding data (Fig. 5). This manner of operation progresses until all of the data have been read out in the column direction and over-written by new data (Fig. 6). See page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
wherein when plural data having written into the memory at present are read in a row direction, plural	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.

data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.		

The following analysis of independent claim 15 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
15. A memory for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that	Fig. 1, 110a; Figs. 4-6	
a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction,	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction;	Figs. 4-6, esp. Fig. 5	Data written in the row direction (Fig. 4) is read out in the column direction; when the first column has been read out, it is over-written by succeeding data (Fig. 5). This manner of operation progresses until all of the data have been read out in the column direction and over-written by new data (Fig. 6). See page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.

plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.		

The following analysis of independent claim 16 is presented for convenience:

Element	Figure(s)	Paragraph(s) and/or page(s)
16. A memory drive apparatus for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that	Fig. 1, 110; Figs. 4-6	
a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction,	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction;	Figs. 4-6, esp. Fig. 5	Data written in the row direction (Fig. 4) is read out in the column direction; when the first column has been read out, it is over-written by succeeding data (Fig. 5). This manner of operation progresses until all of the data have been read out in the column direction and over-written by new data (Fig. 6). See page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.
wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when	Figs. 4-6	Page 15, line 30 to page 16, line 3; page 18, lines 1-14; page 19, lines 8-20.

plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.		

VI. GROUNDS of REJECTION to be REVIEWED ON APPEAL

The issues in the present matter are whether:

1. under 35 USC 102(a), claims 1, 3, 15, 16 and 18 are anticipated by Higashida.

2. under 35 USC 102(a), claims 4, 6, 7 and 9-14 are unpatentable over Higashida in view of Biro.

VII. ARGUMENT

I. Rejection of Claims 1, 3, 15, 16 and 18 as Being Anticipated by Higashida

Higashida discloses a video transfer apparatus that includes interleaving. More than a dozen embodiments are disclosed. Figure 17 relates to a fifth embodiment. Figure 20 relates to a sixth embodiment. Figure 35 relates to an eleventh embodiment. As shown in Figure 15, in the fifth embodiment, interleaving is performed using double-buffering (interleave buffer memory 1002) as is characteristic of the prior art. Likewise in the sixth and eleventh embodiments, as shown in Figure 19 and Figure 33, respectively, interleaving is performed using double-buffering (interleave buffer memories 1002 and 1402, respectively) as is characteristic of the prior art. The only real difference between the interleaving methods of Figures 17 and Figure 20 is how the data is constituted (see col. 23, lines 28-48), not how it is written or read. In the case of Figure 38, because of how the data is constituted in this embodiment, the directions of writing and reading are reversed as compared to Figures 17 and 20.

Parsing the "Response to Arguments" contained in the final rejection, somewhat surprisingly, passages from the reference describing: 1. writing, Embodiment 5; 2. writing, Embodiment 6; 3. writing, Embodiment 11; and 4. reading, Embodiment 5, are concatenated. Not only are the different embodiments "mixed and matched" freely, but the different operations (write and read) of the different embodiments are mixed and matched freely.

Focusing on any particular embodiment of the reference, it may be seen that it is typical of the prior art. Interleaving is performed by writing data into memory in one direction (row or column) and reading data out in the opposite direction. Double

buffering is used to increase throughput. There is no teaching or suggestion of alternating the writing and reading directions so as to avoid the need for double-buffering. That is, there is no teaching or suggestion of "when plural data having [been] written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having [been] written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction" as claimed. Independent claims 1, 15 and 16 therefore are not anticipated by Higashida, nor can dependent claims 3 and 18 be anticipated by Higashida.

I. Rejection of Claims 4, 6, 7 and 9-14 as Being Unpatentable Over Higashida in View of Biro

Whereas Higashida relates to interleaving, the present invention relates more particularly to de-interleaving. Biro teaches de-interleaving.

Biro, however, does nothing to remedy the deficiencies of the primary reference Higashida as distinguished above from the present invention. Accordingly, independent claims 4 and 7 are believed to patentably define over the cited references.

With regard to dependent claims 6 and 9-14, these claims depend from independent claim 1, which has been shown to be patently distinguishable over the cited reference. Accordingly, these claims are also patently distinguishable and allowable over the cited references by virtue of their dependency upon an allowable base claim.

In view of the above, applicant submits that all of the above referred-to claims are patentable over the teachings of the cited references.

VIII. CONCLUSION

In view of the above analysis, it is respectfully submitted that the referenced teachings, whether taken individually or in combination, fail to anticipate or render obvious the subject matter of any of the present claims. Therefore, reversal of all outstanding grounds of rejection is respectfully solicited.

Date: 7/16/07

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IX. APPENDIX: THE CLAIMS ON APPEAL

1. A data writing/reading method of sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

3. A data writing/reading method as claimed in claim 1, wherein plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

4. A method of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in

a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

6. A de-interleaving method as claimed in claim 4, wherein plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

7. A data processing method comprising a first step of interleaving a plurality of data, and a second step of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having

written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

10. A data processing method as claimed in claim 7, wherein the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix form, and contains interleaving the plural data configuring the super frame.

10. A data processing method as claimed in claim 7, wherein the second step is characterize in that interleaved plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

11. A data processing method as claimed in claim 10, wherein the first step is characterized by configuring a super frame having eight frames, each of the frames formed by arranging (203x48) data in matrix form, and is characterized by interleaving (203x48x8) data configuring the super frame, and the second step is characterized in that when (203x48x8) data having written into the memory at present are read in a row direction, (203x48x8) data which is the next to be written are sequentially written in the row direction, on the other hahnd, when (203x48x8) data having written into the memory at present are read in a column direction, (203x48x8) data which is the next to be written are sequentially written in the column direction.

12. A data processing method as claimed in claim 11, wherein the second step is for arranging (203x48x8) data into the memory in 48 matrix structures, each of the 48 matrix structures formed from (203x8) data, and each of the 48 matrix structures is the structure having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

13. A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 26 addresses, and each of the blocks for writing one data into an area corresponding to the one address of each of the blocks, and the second step is for writing one data into the area corresponding to the one address of each of the blocks.

14. A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 4 addresses, and each of the blocks for writing 7 data into an area corresponding to the one address of each of the blocks, and the second step is for writing 7 data into the area corresponding to the one address of each of the blocks.

15. A memory for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first

write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

16. A memory drive apparatus for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

17. A memory drive apparatus as claimed in claim 17, wherein the apparatus provides with addressing means for addressing the memory, and by sequentially addressing the

memory with the addressing means, plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

X. APPENDIX: RELATED PROCEEDINGS

NONE

XI. APPENDIX: EVIDENCE

NONE